| | | | |
|---|---|---|---|
| Peak gate power | $P_{GM}$ | 2 | W |
| Peak pulse voltage ($T_j$=25 ; non-repetitive,off-state;FIG.8) | $V_{pp}$ | 0.5 | kV |

**NOTE 1:** Operating junction temperature $T_j$ is up to 125 when a resistor ≤1kΩ is connected between Gate and Cathode. Without this resistor, the $T_j$ is up to 110 only.

**EECRAIC** $_j$=25 unless otherwise specified) **H**

## [illegible]

J R 02 05 K -/

- J: JieJie Microelectronics Co., Ltd.
- R: Sensitive gate SCRs
- 02: $I_{T(RMS)}$:1A
- 05: $I_{GT}$ ” 200μA
- K: K:TO-252
- -/: Blank:Tube; -TR:Tape & Reel

## [illegible]

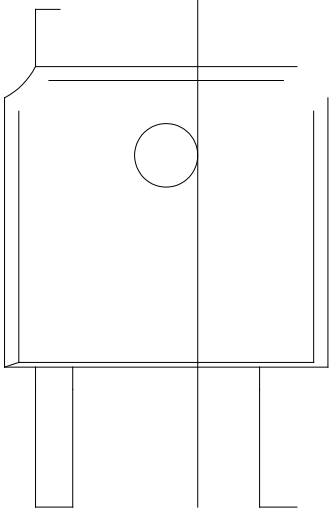


**FIG.1:** Maximum power dissipation versus RMS on-state current



**FIG.2:** RMS on-state current versus case temperature

**FIG.7:** Relative variations of gate trigger current, holding current and latching current versus junction temperature

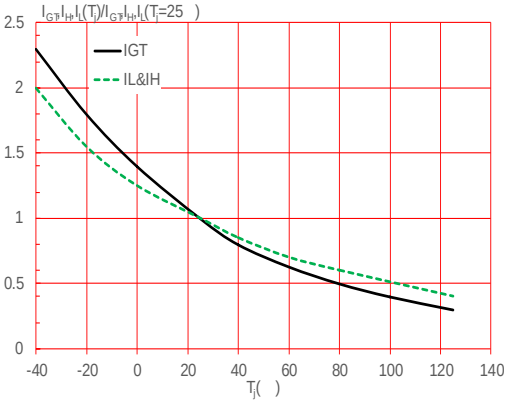
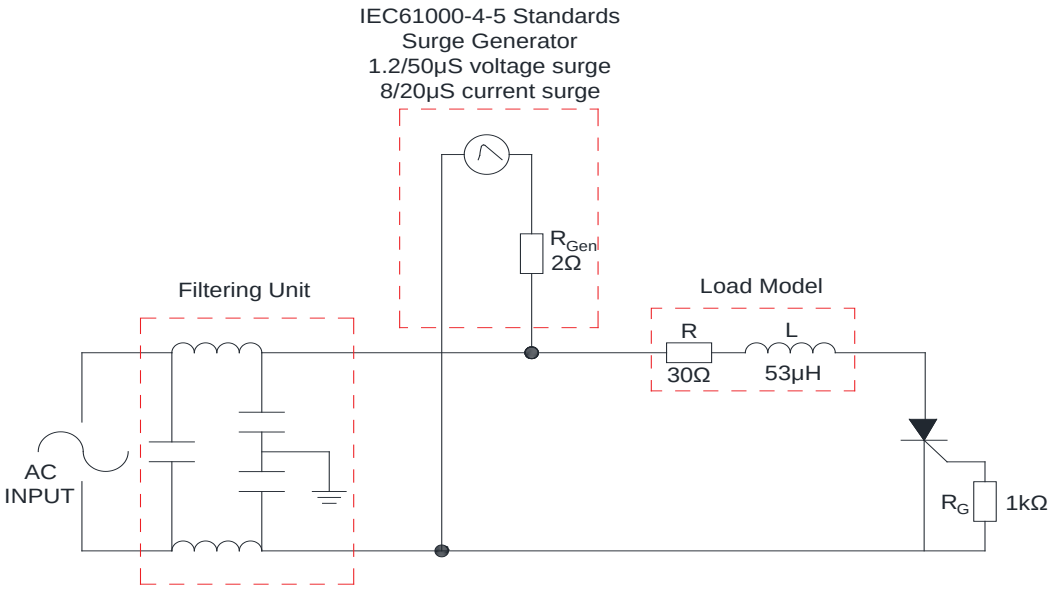
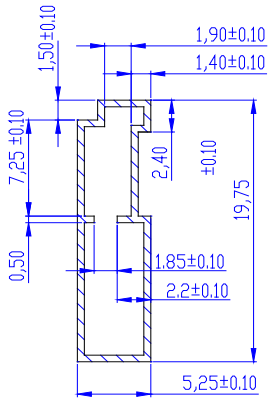


FIG.8 Test circuit for inductive and resistive loads to IEC-61000-4-5 standards



| Order code | Voltage $V_{DRM}/V_{RRM}$ (V) | IGT |
|---|---|---|

DE[redacted]E



Information furnished in this document is believed to be accurate and reliable. However, Jiangsu JieJie Microelectronics Co., Ltd. assumes no responsibility for the consequences of use without consideration for such information nor use beyond it. Information mentioned in this document is subject to change without notice, apart from that when an agreement is signed, Jiangsu JieJie complies with the agreement. Products and information provided in this document have no infringement of patents. Jiangsu JieJie assumes no responsibility for any infringement of other rights of third parties which may result from the use of such products and information. This document supersedes and replaces all information previously